Amendment, claim 9 is amended to obviate the rejection. Accordingly, withdrawal of the rejection is respectfully requested.

The Office Action rejects claims 1-4 under 35 U.S.C. §103(a) over Tsuchiya et al. (U.S. Patent No. 4,729,010), and further rejects claims 5-13 under 35 U.S.C. §103(a) over Tsuchiya in view of Hiraiwa Katsuro (Japanese Patent No. 05-183103). These rejections are respectfully traversed.

In particular, Applicants assert that it would not have been obvious at the time of the invention to modify Tsuchiya using the teachings of Katsuro to teach or suggest a semiconductor device having outer leads that include an upper electrical connecting surfaces on the side of the upper surface of a sealing member, and a lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and where the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane, as recited in independent claims 1, 5 and 9.

Tsuchiya discloses a number of different integrated circuit packages in which semiconductor elements mounted on an insulated substrate can be packaged. See, Abstract. As shown in Figs. 1 and 3-5, the various Tsuchiya devices can include a semiconductor element **1** bonded to an insulating substrate **4** via a metal soldering layer **7**. Various lead pieces **3** are then electrically coupled to the semiconductor element **1** via bonding wires **2**. The semiconductor elements are then encapsulated using a cap **5** and sealing glass layers **6**. See, col. 6, lines 45-59.

Tsuchiya does not teach or suggest a semiconductor device including outer leads that have upper electrical connecting surfaces of a sealing member, and lower electrical connecting surfaces of the sealing member, respectively, and where the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of

the sealing member from the same plane, as recited in independent claims 1, 5 and 9.

To the contrary, Tsuchiya does not even disclose outer leads that have both an upper electrical connecting surface and a lower electrical connecting surface. See, Figs. 1, 3, 4 and 5. As the Tsuchiya leads **3** have only one connecting surface and not both of an upper electrical connecting surface and lower electrical connecting surface, there can be no possible way to gauge both the plane formed by a lower surface against the height of an upper surface. Thus, Tsuchiya does not teach or suggest each and every limitation of independent claims 1, 5 and 9.

Katsuro discloses a semiconductor device and package designed such that a plurality of chips can be piled atop each other in multiple stages. See, Purpose. As shown in the accompanying figure, electrode leads **6**, side-notch leads **7** and electrode leads **8** are formed on a printed circuit board **1** after which memory chips **2** and inner leads **5** can then be subjected to wire bonding and resin sealing. A recess **9** for receiving a sealing resin **3** is then formed on the side of the circuit board **1** opposite of the side of the memory chip **2**. Katsuro does not teach or suggest a semiconductor device including outer leads that have a height from a plane including the lower surface of a sealing member greater than that of the upper surface of the sealing member from the same plane.

To the contrary, as clearly shown in the figure, while the Katsuro device does include wiring leads (**6**, **7**, **8**) that together wrap around printed circuit board **1**, at no point do the combined leads (**6**, **7**, **8**) ever rise above the sealing resin **3**. As a result, when Katsuro devices are stacked, heat is apt to accumulate in the memory circuit chip die, thus lowering device reliability. See, page 2, line 25 to page 3, line 10 of the specification. Thus, Katsuro does not provide for the deficiencies of Tsuchiya.

The Office Action has not established a *prima facie* case of obviousness. To establish a

prima facie case of obviousness, the prior art references must teach or suggest all the claim limitations, and there must be some motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the reference teachings. See MPEP §2143, for example. As discussed above, Tsuchiya and Katsuro, individually or in combination, do not teach or suggest a semiconductor device including outer leads that have a height from a plane including the lower surface of a sealing member greater than that of the upper surface of the sealing member from the same plane, as recited in independent claims 1, 5 and 9.

Furthermore, there is no motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Tsuchiya using the teachings of Katsuro. While the Office Action asserts that "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a sealing member, since the sealing member can be used to seal semiconductor elements", nowhere is this disclosed or suggested in the applied art of record. Still further, assuming that it would have been obvious to substitute the seal of Katsuro for the lid of Tsuchiya (a proposition contested by Applicants), this does not address any motivation necessary to modify either of Katsuro and Tsuchiya to include devices having appropriately configured outer leads.

Thus, independent claims 1, 5 and 9 define patentable subject matter. Claims 2-4, 6-8 and 10-13 define patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejection of claims 1-13 under 35 U.S.C. §103(a) is respectfully requested.

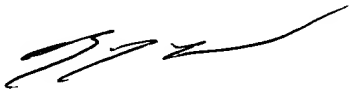
For the reasons given, Applicants believe that this application is in condition for allowance and Applicants request that the Examiner give the application favorable consideration and permit it

to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representative listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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Appendix Showing Claim Changes

Claim 9 is amended as follows:

9. (Amended) A semiconductor device comprising:

a printed wiring board; and

[a semiconductor package,] a plurality of semiconductor packages mounted on the printed wiring board [with a] , each semiconductor package having an upper surface of a sealing member thereof facing the printed wiring board and outer leads thereof connected to electrodes formed on the printed wiring board; wherein each of the plurality of semiconductor packages comprises,

a die pad;

a die mounted on the die pad;

outer leads electrically connected to electrodes of the die by bonding wires, respectively; and

the sealing member sealing therein the die, the bonding wires, parts of the outer leads and a part of the die pad, and having the upper surface on the side of the die and a lower surface on the side of the die pad;

wherein the outer leads have upper electrical connecting surfaces on the side of the upper surface of the sealing member, and lower electrical connecting surfaces on the side of the lower surface of the sealing member, respectively, and the outer leads have a height from a plane including the lower surface of the sealing member greater than that of the upper surface of the sealing member from the same plane.